



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/581,117

05/30/2006

Jozef Pieter Van Gassel

NL 031406

5189

24737

7590

02/26/2009

PHILIPS INTELLECTUAL PROPERTY & STANDARDS

P.O. BOX 3001

BRIARCLIFF MANOR, NY 10510

EXAMINER

SNYDER, STEVEN G

ART UNIT

PAPER NUMBER

2184

MAIL DATE

DELIVERY MODE

02/26/2009

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/581,117	<b>Applicant(s)</b> VAN GASSEL ET AL.	
	<b>Examiner</b> STEVEN G. SNYDER	<b>Art Unit</b> 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 December 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 9-14 and 20 is/are rejected.
- 7) ☒ Claim(s) 4-8 and 15-19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Appeal Brief***

In view of the Appeal Brief filed on December 5, 2008, PROSECUTION IS HEREBY REOPENED. The Office Action with the new ground(s) of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

- (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
- (2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1 to 20 have been considered but are moot in view of the new grounds of rejection.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**3. Claims 1 – 2, 9 – 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olsen et al., U.S. Patent Application 2005/0071561 (hereinafter referred to as Olsen) in view of Kever et al., U.S. Patent Application 2003/0145239 (hereinafter referred to as Kever).**

**Referring to claim 1**, Olsen discloses “A method for adaptively minimising the total power consumption of an apparatus comprising a subsystem comprising a mass storage device and a buffer memory” ([0006], using a DRAM reduces energy consumption by eliminating Hard-disk drive (HDD) accesses), said method comprising the steps of “determining an optimum buffer size for which the power consumption of said subsystem is a minimum” ([0008], efficiently managing available capacity of a cache is important for power consumption and [0028], managing levels of storage hierarchy by limiting cache usage to specific parts) “for a given streaming bit-rate to/from said buffer memory” ([0028] and [0035], current throughput demands. Throughput is defined in [0021] as data per unit time).

As stated above Olsen discloses efficiently managing available capacity of a cache for power consumption of a system.

Olsen does not appear to explicitly disclose how the capacity is managed. Therefore Olsen does not appear to explicitly disclose “adjusting the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal.”

However, Olsen does disclose that “it is known that accessing a main storage device such as an HDD 106 consumes more energy than accessing information stored in random-access media such as the main memory 104” in [0025].

Kever discloses a method for saving power consumed by cache memory ([0007] – [0008]). In this method sections are turned on or off depending on needs of the system.

Olsen and Kever are analogous art because they are from the same field of endeavor, which is power saving in a storage system.

Therefore, through the teachings of Olsen (reducing energy utilized by an HDD by using buffer memory) and the teachings of Kever (reducing the energy utilized by cache memory by resizing the cache according to system needs), it would have been obvious to one of ordinary skill in the art at the time of the invention to find an “optimal” buffer size for a system’s current throughput needs.

The motivation for doing so would have been to reduce power utilized by the HDD (as described by Olsen) while also minimizing power utilized by the buffer itself (as described by Kever).

Therefore, it would have been obvious to combine Kever with Olsen to obtain the invention as specified in the instant claim.

**As per claim 2**, Olsen discloses efficiently managing available capacity of a cache is important for power consumption and managing levels of storage hierarchy by limiting cache usage to specific parts ([0008] and [0028]).

However, Olsen does not appear to explicitly disclose “said step of adjusting the buffer size comprises switching on memory banks and/or memory ICs of said buffer memory for increasing the size of said buffer memory, and switching off memory banks and/or memory ICs for decreasing said buffer memory.”

However, Kever discloses switches used to control whether or not each memory array is powered on or off (Figs. 1 and 2).

Olsen and Kever are analogous art because they are from the same field of endeavor, which is power saving in a storage system.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Olsen and Kever before him or her, to modify the teachings of Olsen to include the teachings of Kever so that memory buffer banks would be switched on and off to dynamically change the buffer size.

The motivation for doing so would have been to minimize power utilized by the buffer memory to coincide with efforts to reduce power utilized by the HDD in an attempt to find an “optimal” buffer size (as stated above).

Therefore, it would have been obvious to combine Kever with Olsen to obtain the invention as specified in the instant claim.

**Referring to claim 9**, claim 1 recites corresponding limitations as that of claim 9. Therefore, the rejection of claim 1 applies to claim 9. Further limitations of claim 9 are discussed below.

Olsen discloses the circuit comprising “a processing unit” (Fig. 1, processor 102) and “retrieve the data from the mass storage device” ([0006], HDD and using DRAM as a read cache).

**As per claim 10**, Olsen discloses “An apparatus comprising a subsystem comprising mass storage device, a buffer memory” (Fig. 1, main storage device 106, main memory 104) “and the circuit according to claim 9 (see rejection to claim 9 and claim 1 above).

**As per claim 11**, Olsen discloses efficiently managing available capacity of a cache is important for power consumption and managing levels of storage hierarchy by limiting cache usage to specific parts ([0008] and [0028]).

However, Olsen does not appear to explicitly disclose how the capacity is managed. Therefore Olsen does not appear to explicitly disclose “said buffer memory comprises SDRAM circuits having banks of memory adapted to be independently switched on/off.”

However, Olsen does disclose that “it is known that accessing a main storage device such as an HDD 106 consumes more energy than accessing information stored in random-access media such as the main memory 104” in [0025]. Also, Olsen discloses tradeoffs among memory types including SRAM and DRAM ([0007]).

Kever discloses a method for saving power consumed by cache memory ([0007] – [0008]). In this method sections are turned on or off depending on needs of the system.

Olsen and Kever are analogous art because they are from the same field of endeavor, which is power saving in a storage system.

Therefore, through the teachings of Olsen (reducing energy utilized by an HDD by using buffer memory) and the teachings of Kever (reducing the energy utilized by cache memory by resizing the cache according to system needs), it would have been obvious to one of ordinary skill in the art at the time of the invention to find an “optimal” buffer size for a system’s current throughput needs.

The motivation for doing so would have been to reduce power utilized by the HDD (as described by Olsen) while also minimizing power utilized by the buffer itself (as described by Kever).

Therefore, it would have been obvious to combine Kever with Olsen to obtain the invention as specified in the instant claim.

**As per claim 12**, Olsen discloses “a scheduler function executable by the processing unit controls accessing the storage device and the buffer memory” ([0024] and Fig. 1, arbiter or storage controller 116).

**Referring to claim 13**, Olsen discloses a “subsystem comprising a mass storage device and a buffer memory” (Fig. 1, main storage device 106 and main memory 104).



Olsen does not appear to explicitly disclose “A computer-readable medium having embodied thereon a computer program for processing by a computer, the computer program comprising code segments for adaptively minimising the total power consumption of a subsystem comprising a mass storage device and a buffer memory, wherein a first code segment determines an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate from said buffer memory, and a second code segment adjusts the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal.”

However, Kever discloses an application sending signals to instruct the switching on and off of memory sections ([0010]). Also, Kever discloses a microprocessor monitoring the system and switching memory sections on and off ([0005]).

Also, Olsen does disclose that “it is known that accessing a main storage device such as an HDD 106 consumes more energy than accessing information stored in random-access media such as the main memory 104” in [0025].

Kever discloses a method for saving power consumed by cache memory ([0007] – [0008]). In this method sections are turned on or off depending on needs of the system.

Olsen and Kever are analogous art because they are from the same field of endeavor, which is power saving in a storage system.

Therefore, through the teachings of Olsen (reducing energy utilized by an HDD by using buffer memory) and the teachings of Kever (reducing the energy utilized by

Art Unit: 2184

cache memory by resizing the cache according to system needs), it would have been obvious to one of ordinary skill in the art at the time of the invention to find an “optimal” buffer size for a system’s current throughput needs.

The motivation for doing so would have been to reduce power utilized by the HDD (as described by Olsen) while also minimizing power utilized by the buffer itself (as described by Kever).

Therefore, it would have been obvious to combine Kever with Olsen to obtain the invention as specified in the instant claim.

**Note, claim 20** recites the corresponding limitations of claim 12. Therefore, the rejection of claim 12 applies to claim 20.

**4. Claims 3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olsen in view of Kever, as applied to claims 1 – 2, 9 – 13, and 20 above, and further in view of Gibbs et al., U.S. Patent Application 2002/0045961 (hereinafter referred to as Gibbs).**

**As per claim 3**, Olsen discloses “the storage device is a harddisk drive” ([0006], using a DRAM reduces energy consumption by eliminating Hard-disk drive (HDD) accesses). Olsen also discloses taking current throughput demands into consideration ([0028] and [0035], current throughput demands)

Art Unit: 2184

As stated above, through the teachings of Olsen (reducing energy utilized by an HDD by using buffer memory) and the teachings of Kever (reducing the energy utilized by cache memory by resizing the cache according to system needs), it would have been obvious to one of ordinary skill in the art at the time of the invention to find an “optimal” buffer size for a system’s current throughput needs.

The motivation for doing so would have been to reduce power utilized by the HDD (as described by Olsen) while also minimizing power utilized by the buffer itself (as described by Kever).

However, neither Olsen nor Kever appears to explicitly disclose “the step of determining an optimum buffer size comprises determining a harddisk drive data rate, determining the stream bit-rate to/from the buffer memory, and determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate.”

Gibbs, however, discloses deciding to activate a storage device depending on factors such as the data transfer rate of the storage device and a data sample rate ([0034]).

Olsen, Kever, and Gibbs are analogous art because they are from the same field of endeavor, which is power saving in a storage system.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Olsen, Kever, and Gibbs before him or her, to modify the teachings of Olsen and Kever to include the teachings of Gibbs so that a current data sample rate and a data transfer rate of a storage device would be factors for

Art Unit: 2184

adjusting a buffer size when attempting to find an ideal system in terms of power consumption.

The motivation for doing so would have been to provide a method for power saving that changes dynamically with data throughput changes.

Therefore, it would have been obvious to combine Gibbs with Olsen and Kever to obtain the invention as specified in the instant claim.

**Note, claim 14** recites the corresponding limitations of claim 3. Therefore, the rejection of claim 3 applies to claim 14.

#### ***Allowable Subject Matter***

5. **Claims 4 – 8, 15 – 19** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Application **2004/0062119** discloses dynamically managing memory for minimizing power.

U.S. Patent **6,684,298** discloses dynamically reconfigurable memory for optimizing speed and power.

U.S. Patent Application **2007/0136522** discloses varying a buffer's capacity for power consumption purposes.

U.S. Patent Application **2004/0215986** discloses dynamic power management by varying data rate.

### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN G. SNYDER whose telephone number is (571)270-1971. The examiner can normally be reached on Mon. - Thurs. 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2184

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven G Snyder/  
Examiner, Art Unit 2184

**/Henry W.H. Tsai/  
Supervisory Patent Examiner, Art Unit 2184**